ABSTRACT OF THE INVENTION

In a CMOS basic cell used in fabrication of a gate array semiconductor integrated circuit, each of the gate and the diffusion region of a P-channel transistor is in a hooked shape having bent parts respectively bending to the left and right at the upper and lower portions thereof. Similarly, each of the gate and the diffusion region of an N-channel transistor is in a hooked shape having bent parts respectively bending to the left and right at the upper and lower portions thereof. In the case where a semiconductor integrated circuit is fabricated by arranging basic cells having the same structure on the right and left hand sides of this basic cell, the basic cells adjacent to each other are overlapped by portions thereof corresponding to one grid, so that the portions in the hooked shapes can be alternately inlaid with each other. Accordingly, the semiconductor integrated circuit attains a smaller layout area.